Ivan Feňo - Eduard Jadroň - Pavol Špánik *

RIADIACE OBVODY PRE SÉRIOVÝ, ČIASTOČNE REZONANČNÝ MENIČ

CONTROL CIRCUITRY FOR A PARTIAL SERIES RESONANT CONVERTER

Príspevok predkladá riešenie riadiaceho obvodu pre nový vysokofrekvenčný DC-DC menič vhodný pre aplikácie vo výkonovom rozsahu niekoľko kilowatov. Zapojenie výkonovej časti meniča je založené na sériovom polomostovom rezonančnom meniči. Rezonančný jav sa vyskytuje len počas časti periódy činnosti meniča. Počas každej polperiódy meniča sa transformuje na sekundárnu časť diskrétny energetický impulz. Tým je umožnené riadenie meniča zmenou jeho pracovnej frekvencie. Menič sa vyznačuje spínaním pri nulovom napätí (ZVS) a vypínaním pri redukovanom prúde pre hlavné polovodičové spínače a komutáciou pri nulovom prúde pre usmerňovacie diódy. Tieto vlastnosti predurčujú menič pre IGBT, pričom sa môže dosiahnuť vyššia pracovná frekvencia s relatívne pomalými prvkami. Predpokladaná účinnosť meniča je vysoká počas malej aj veľkej záťaže, pričom rozsah výstupného napätia je dvojnásobný oproti konvenčnému polomostovému sériovému rezonančnému meniču. Jadro článku pozostáva z PSpice modelov jednotlivých častí meniča a zo simulačných výsledkov, ktoré boli dosiahnuté ich použitím.

A control circuit for a new high-frequency DC-DC converter, suitable for application in a few kilowatts range, is presented. The converter topology is based on a half bridge series resonant converter, i. e. having only two switches. Resonance occurs only for a part of each switching cycle, and a discrete energy pulse is transferred to the load every half cycle, rendering a variable frequency controller for controlling the output power. The converter features zero-voltage turn-on and snubbed turn-off at reduced current for the switching devices, and zero current commutation of the rectifier diodes, making it suitable for IGBT switches operating at a switching frequency higher than 20 kHz. The efficiency of the converter is supposed very high under full load and low load conditions, while the dynamic output voltage range is two times larger than that of the conventional half bridge Series Resonant Converter. PSpice Model presents the entire converter and control circuit.

1. Introduction

In a number of applications, such as battery chargers and traction, the static power converter operates at full load for a small proportion of an operating cycle. Though most full load efficiencies are high in modern switch mode power converters, the efficiency drops significantly under small load conditions, and the overall efficiency over the full cycle can be low. This phenomenon can be attributed to transformer magnetization losses, switching losses, and for most resonant and/or soft switching converters, additional conduction losses due to circulating currents. In addition, when charging totally discharged batteries, the voltage must be increased, and a specified current has to be provided before the voltage reduces to its normal value and full load current is applied. Commercial battery chargers (50/60 Hz ferro-resonant technology) cannot provide any current at a sufficiently large voltage, and it is consequently not possible to charge batteries in the mentioned condition. Furthermore, if a square wave converter such as a half bridge converter should be used and be designed to provide a sufficiently high output voltage, it will operate under a low switching duty cycle at full power output. This will lead to poor full load efficiency because of the bad utilization of the semiconductor switches, especially when using MOSFET's. This problem is also commonly encountered with modern DC welding power supplies, where a high voltage is required to draw an arc, while a lower output voltage is required during welding.

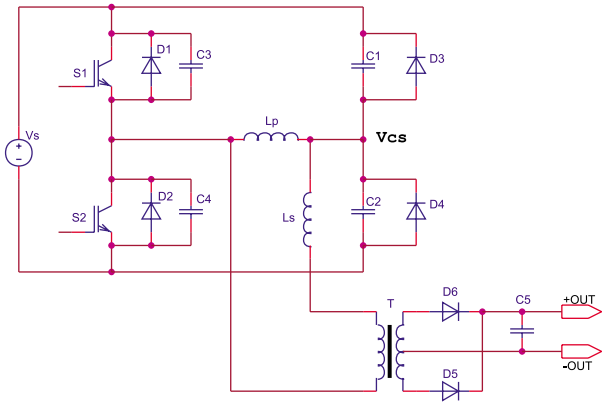

Fig. 1 Power circuit

* **MSc. Ivan Feňo, MSc. Eduard Jadroň, Associate Professor Pavol Špánik, PhD.**
Department of Electrical Traction and Energetics, Faculty of Electrical Engineering, University of Žilina, Veľký diel, 010 26 Žilina, Slovak Republic,
Tel.: +421-41-565 2231, 565 2231, 513 2175
E-mail: feno@kete.utc.sk, ej@edo.spsmt.sk, spanik@fel.utc.sk

2. The ZVS Partial Series Resonant Converter (PSRC)

The PSRC is a new variation of the well-known Series Resonant Converter (SRC) in the half bridge configuration. The only topological differences are the addition of a clamping diode parallel to each of the two resonant capacitors, and the inclusion of a parallel inductance *Lp*, as shown on Fig. 1. The clamped capacitor voltage limits the voltage stresses of the capacitors, which is an important improvement regarding cost and reliability, especially at higher power levels.

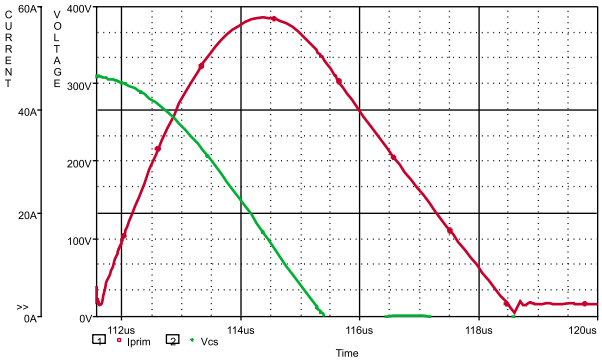

Fig. 2 Voltage Vcs and Iprim current in PSRC circuit

The additional parallel inductance *Lp* is used to commutate voltage *Vd* when both switches (*S*1 and *S*2) are turned off, and therefore obtaining ZVS. In the conventional SRC, ZVS can only be achieved with the switching frequency always higher than the resonant frequency of the resonant tank (*L* and *C*).

This requires either a high switching frequency or large reactive components, when considering that the switching frequency has to be varied over a large range to have sufficient control of the output power, with the minimum switching frequency at 20 kHz. The PSRC, however, achieves ZVS with the switching frequency always lower than the resonant frequency of the resonant tank (*C*1, *C*2 and *Ls* in Fig. 1), resulting in a significant reduction in size of the reactive components, and of the transformer.

Switching conditions are very favorable for diodes *D*3 and *D*4, since the large resonant capacitors, *C*1 and *C*2, effectively act as snubbers. The rectifier diodes, *D*5 and *D*6, experience very low switching losses due to the sinusoidal transformer current, resulting in soft switching for all semiconductor devices in the power circuit. Therefore, slower and cheaper devices could be used at high switching frequency ($>$ 50 kHz).

The main feature of the ZVS PSRC operation is the fact that *Vcs* swings from *Vs* to zero volts, or vice versa, during every half-switching cycle. The resulting voltage and current waveforms for the half-switching cycle with *S*2 being switched on are as shown in Fig. 2. Note that the initial condition for *Vcs* for this particular half-switching cycle is $Vcs = Vs$.

The first part of a switching cycle consists of a resonance interval with current being conducted by the two resonant capacitors (*C*1 and *C*2), *Ls*, *Lp* and *S*2. First part is followed by the discharging interval during which the energy stored in *Ls* is discharged into the combination of *C*5 and the output. Lastly, there is the freewheeling interval during which *S*2, *D*4 and *Lp* only conduct current. Turn-off of *S*2 can occur during the freewheeling

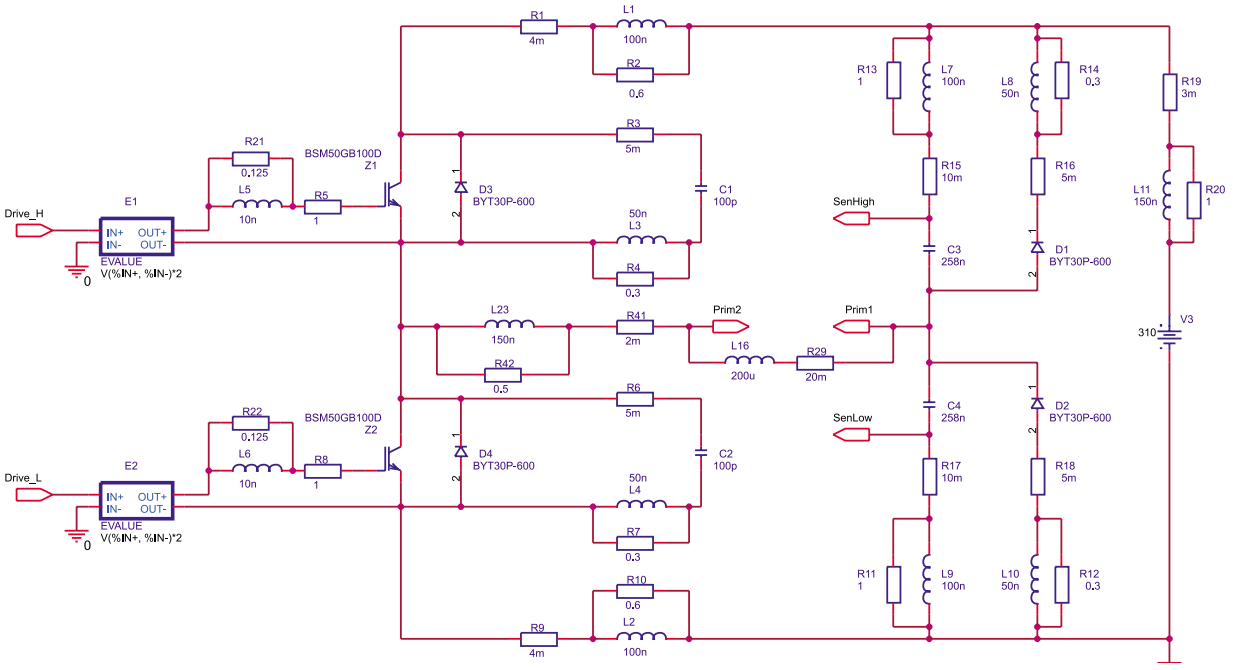

Fig. 3 Primary part simulation model schematic

interval, with commutation of the switch current to *C*3 and *C*4, resulting in low turn-off losses. *C*3 and *C*4 will therefore conduct Iprim until *D*1 clamps *Vd* to *Vs* and *S*1 can then be turned on, obtaining ZVS. All the energy stored in the resonant capacitors, *C*1 and *C*2, will therefore be transferred to the output each time the two switches are commutated (i.e. every half-switching cycle). This results in the (1) equation for the output power, where *fs* is the switching frequency. The average output power is controlled by simply varying the switching frequency, provided that *Vcs* does a full excursion between the positive and the negative supply during each half switching cycle, while *C*1 and *C*2 resonate predominantly with *Ls*.

$$P_{OUT} = (C_1 + C_2)V_S^2 f_S \qquad (1)$$

The latter implies that the output voltage *Vout* must be lower than half the supply voltage *Vs*, when assuming normalized transformer turns ratio. The parallel inductance *Lp* is much larger than the series inductance *Ls*. Inductors, *Ls* (the leakage inductance) and *Lp* (the magnetizing inductance), and the transformer (T) are integrated into one physical structure, resulting in a minimum number of components.

At high output voltages, i.e. when *Vcs* > *Vs*/2, *Vcs* is partly resonated by *Lp* at reduced frequency, and the output power is therefore reduced. Under no load conditions, *Vcs* is commutated by *Lp* alone, and the output vo1tage *Vout* is then equal to the supply voltage *Vs*, divided by the transformer turns ratio.

3. The Control Circuit Description

Based on operational principles and welding requirements, control circuit has been designed and all the power part and control part simulation models has been built for PSpice A/D software. Fig. 5 presents control part, Fig. 3 shows primary power part and secondary part is shown on Fig. 4. To “time” the circuit, voltage controlled ramp generator is used that employs operational amplifier integrator. When ramp reaches certain voltage level, a comparator changes its state and switching devices commutation can occur. In this moment, ramp generator is reset and next cycle starts

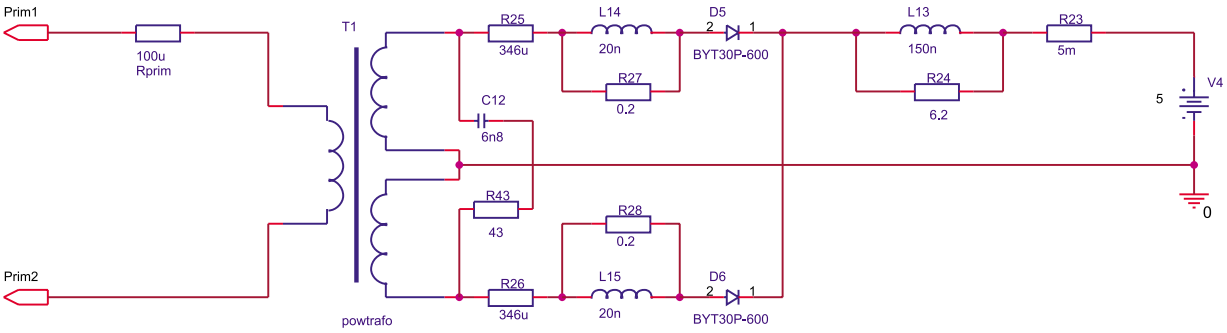

Fig. 4 Secondary part simulation model schematic

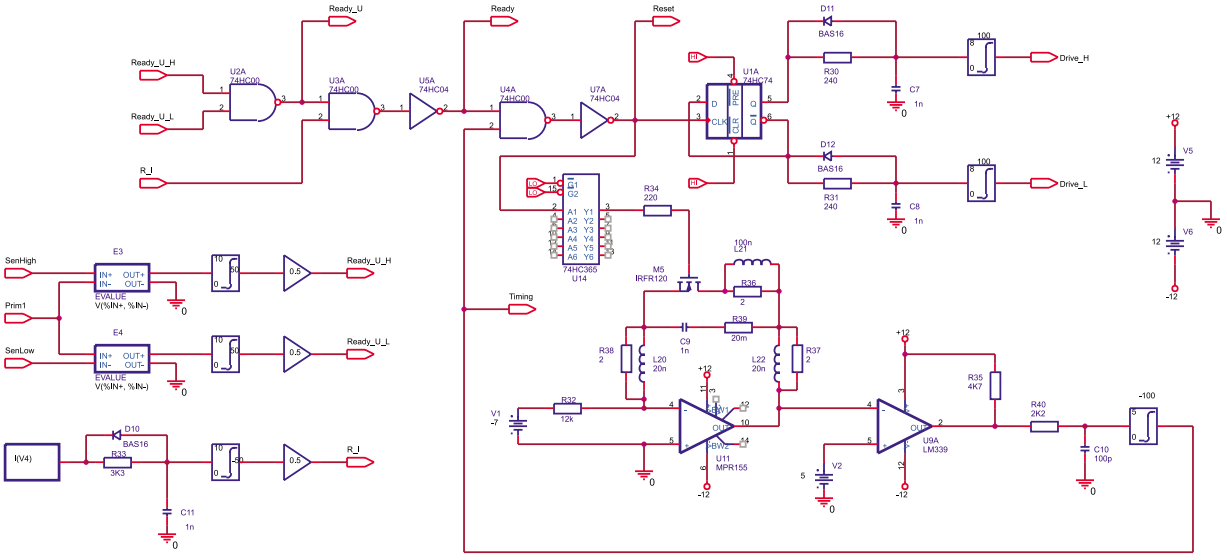

Fig. 5 Control part simulation model schematic

circuit timing. The slope of the ramp is defined by control voltage that in turn determines switching frequency, and hence, output power of the converter.

However, in the case of light load condition, *Vcs* voltage doesn't exhibit full transient from *Vs* to zero (and vice versa) before timing is finished and, hence, commutation has to be delayed to obtain a full energy pulse conversion. Therefore, the circuit features a voltage checking part, which tracks *Vcs* voltage (Fig. 5, 3). Due to this fact, a reset signal for the ramp generator is gated by "Ready-V" signal. *Vcs* checking part that has been mentioned above provided this signal.

Next, in a heavy load condition, output current doesn't decrease so fast and circuit timing is finished before current in power switches decays to zero. The circuit has therefore next watching part for output current tracking which generate "Ready-I" signal. This signal provides delay to ramp reset too and ensures zero current state for commutation.

4. Circuit waveforms

A simulation model for power circuit consisting of a primary and secondary power part in conjunction with a control circuit has been designed and built for PSpice A/D software.

Left side part on Fig. 6 shows Vcs voltage and rectified current (rectifier diodes current sum). Right side part presents voltage across and current through *S*1. Waveforms are valid for output voltage equaled to 0.31 times supply voltage *Vs* (transformer turns ratio $N1/N2 = 4$). In this case $Vs = 310$ V, $Vout = 24$V, $Iout = 97$ A, switching frequency $fs = 55$ kHz. Peak switch current reaches 58 A; voltage across switch doesn't pass 320 V. Peak output rectifier current reaches 215 A; current downslope value is 55 A/μs. A commutation interval is determined by timing circuit therefore switching frequency is constant if load is lightly changed.

Fig. 7 presents the same waveforms as previous figure but output voltage *Vout* is forced to 5 V. Other values are $Vin = 310$ V, $Iout = 135$A, switching frequency fs is set to 26 kHz by current tracking circuit that delays reset signal for integrator circuit since switch current decays slowly. Peak switch current reaches 72 A; voltage across switch doesn't pass 321 V. Peak output rectifier current reaches 283 A; current downslope value is 21A/μs.

Fig. 8 shows the waveforms for output voltage *Vout* forced to 60 V. Other values are $Vin = 310$ V, $Iout = 19$ A, switching frequency fs is 26.1 kHz due to voltage tracking circuit that checks *Vcs* for full swing from *Vs* to zero and vice versa. Peak switch current is 18 A; voltage across switch doesn't pass 320 V. Peak output rectifier current reaches 85A; current downslope value is 39A/μs.

5. Conclusion

The Zero Voltage Switching Partial Series Resonant Converter provides the following advantages for use in arc welding applications, when being compared with present technology being used in commercial inverter welders:

- High open circuit voltage, equa1 to the supply voltage *Vs* when assuming a normalized transformer turns ratio.
- 50 % switching duty cycle with an output voltage lower than half *Vs*, with normalized transformer turns ratio.
- Very low conduction and switching losses due to ZVS, and sinusoidal switch current, resulting in snubbed turn-off at reduced current
- Obtain ZVS with the switching frequency lower than the resonant frequency, reducing the size of all the active components, including the transformer.
- Sinusoidal transformer current, minimizing copper losses.
- Low switching losses for the clamping diodes and for the rectifier diodes, further reducing semiconductor losses.
- Naturally constant power load line when the output voltage is less than half *Vs* (normalized transformer turns ratio).

In contrast to almost all commercial DC welders, the output of the PSRC is derived from a capacitor. This results in the fastest possible current rise rate at arc initiation, because the inductance of the welding cables is the only component that limits the rate of rise of the output current.

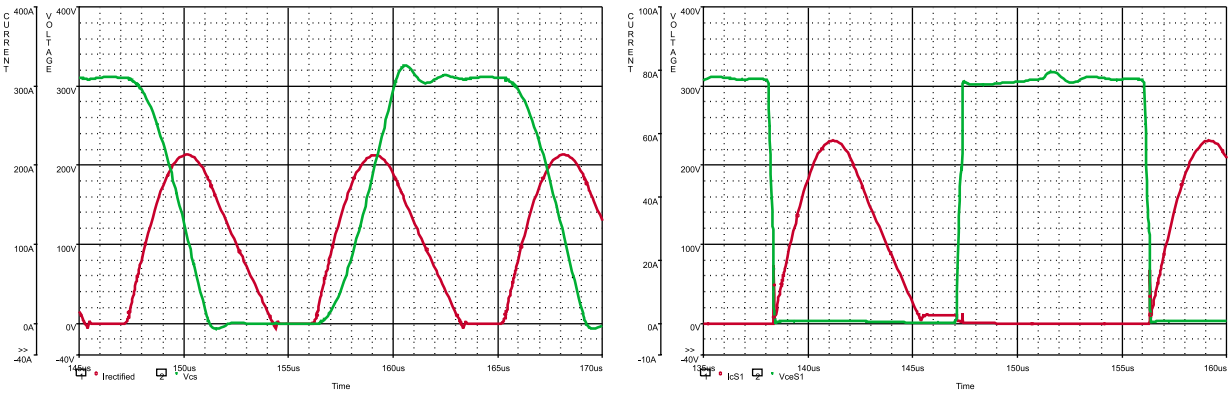

Fig. 6 Key waveforms for Vout = 24 V

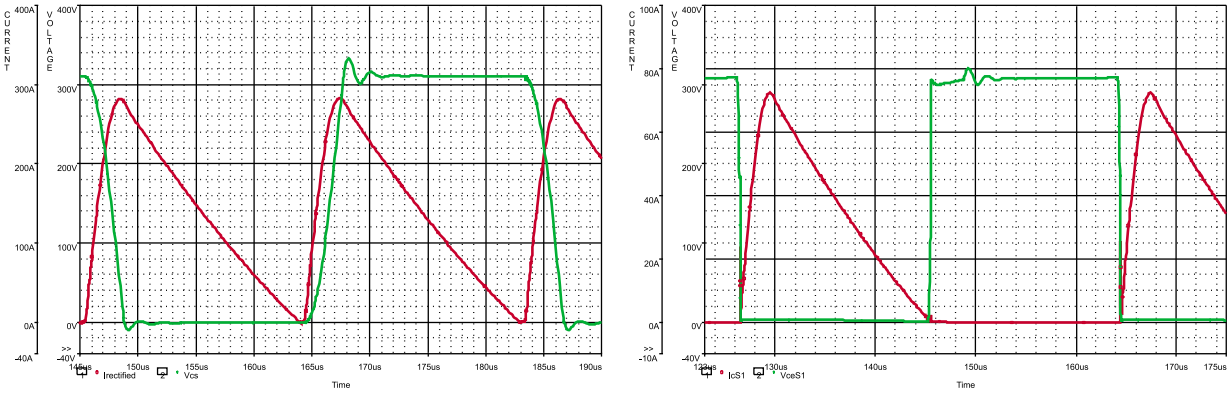

Fig. 7 Key waveforms for Vout = 5 V

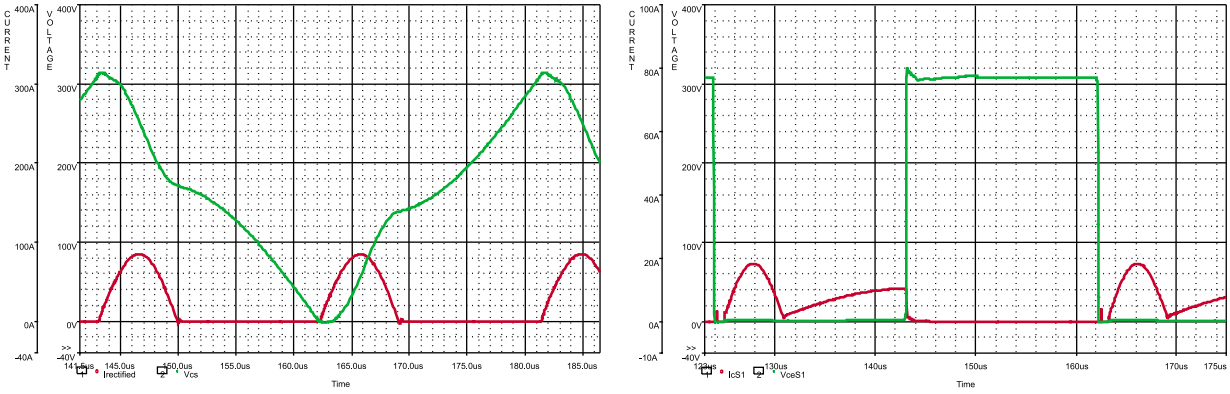

Fig. 8 Key waveforms for Vout = 60 V

6. References

[1] Theron, P. C., Ferreira, J. A.: *"A new Partial Series Resonant Converter for efficient DC to DC conversion"* PCC Yokohama Proceedings, Tokio, Japan, April 1993, pp 171-176

[2] Theron, P. C., Ferreira, J. A.: *"The Partial Series Resonant Converter: A new DC to DC converter with good light load efficiency"*. IEEE-IAS Conference, 1993

[3] Kováčová, I., Kováč, D.: *Výkonové tranzistory MOSFET a IGBT*, ELFA, Košice 1996

[4] Dzurko, P., Dudrík, J., Vyšnyi, P.: *"Behavior of Arc Welder with high frequency LCC resonant Converter"*, EPE-PEMC – 2000 Conference, Košice