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## ISSUES IN DESIGNS OF HIGH CURRENT APPLICATIONS

*This paper deals with design high current printed circuit boards (PCB), with the issues of implementation the power layer into standard PCB and influence of parasitic parameters of conductive traces of PCB. The parasitic parameters of conductive traces play a significant role in design of high current PCB, and therefore must be minimized. The technology of manufacturing PCB for high current designs as a compact device is mentioned in the paper. The quality of MOSFET switching power in high current design was compared in two ways of proposed leading power lines in order to demonstrate the influence of parasitic inductances of conductive traces.*

**Keywords:** automotive, high current, printed circuit board

### 1. Introduction

Automotive industry is one of the fastest developing kind of industry. It is characterized by high requirements on reliability and safety of all devices. The important sign of automotive industry is voltage power supply, 12 volts for personal cars and 24 volts for trucks.

Modern trend of automotive area is set on the replacement of less reliable, usually mechanical systems by more reliable and smarter electrical systems. The electric turbocharger, power steering or electric assisted parking brake are modern electrical systems based on principle, as were the previous mechanical systems [1 - 3]. These electrical systems are usually driven by 3-phase PMSM motors and they are supplied by high performance inverter.

There are many important factors in development of high current application. Three key factors of high current applications development will be mentioned, which are needed to be solved. First factor relates minimizing of parasitic inductances of design, due to influence on quality of switching, and total electromagnetic interference of design. Second factor relates to thermal performance of the design. That means, minimizing of generated heat, dissipation of heat and cooling. Third factor relates to feasibility of manufacturing of the design, in terms of dimensions limitations.

The geometry and the material of the PCB have impact on the thermal performance of the high current design. This influence of material and geometry of PCB on thermal performance of design is mentioned in [4].

In order to minimize parasitic inductances and reaching good thermal performance, the optimization of layout is mentioned in [5]. The authors have developed high current power converter design for three-phase motors and investigate the influence of parasitic inductances on the quality of switching and thermal performance.

In the end, it is necessary to mention, that the automotive industry is targeting low cost and high efficiency designs. With the growing market of electrical vehicles, the efficiency of the devices will play the key role of the development.

### 2. Topology of the printed circuit boards for high current applications

Function of printed circuit board (PCB) in electronics is physical and electrical connection of the components, forming an electronic device. The main challenge of high current PCB, is necessity to withstand flow of current and to ensure that the device would work in standard and safe operation. The design approach of PCB for high current application is mentioned in [6]. The authors propose making multilayer power board with stack of power layers. Advanced method of manufacturing the PCB for high current applications is called Iceberg. This technology was patented by KSG Leterplatten GmbH company. Iceberg technology allows to design the conductive layer with different thickness. This technology is suitable for compact devices to source high current loads. The mechanical and electrical

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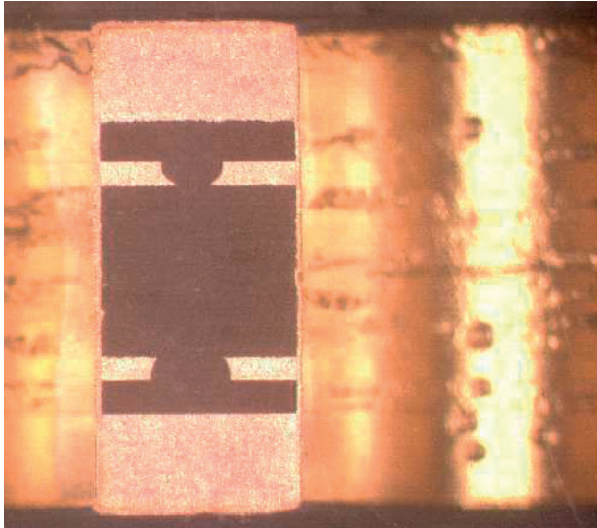


Figure 1 Cross section of four layers PCB made by Iceberg technology with power layers on outer side

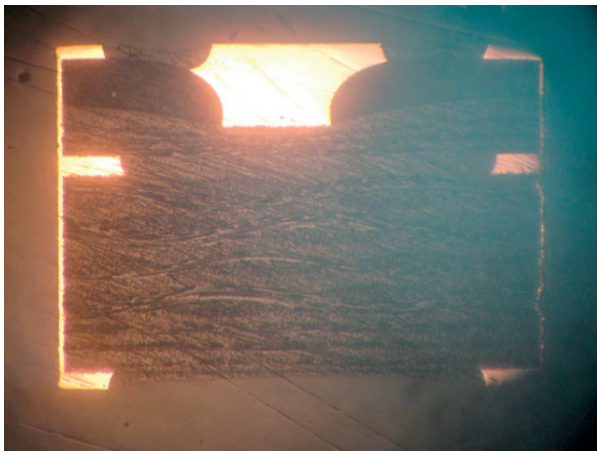


Figure 2 Cross section of four layers PCB made by Iceberg technology with one layer of power line on outer side

components signal or power circuits are integrated on the same side of PCB [7].

The designer has two possibilities of designing the PCB with Iceberg technology. The first design defines the thickness of conductive material for one layer of PCB. The thickness of conductive layer can be determined for leading of high density of current, or can be determined for conductive connection of signal circuits.

Figure 1 shows a cross section of 4 layers PCB with implementation 400  $\mu\text{m}$  thickness of conductive layer on both outer layers of PCB. This power conductive layer can be also implemented on one outer layer of PCB only, while the thickness of other layers can be different. The cross section of this PCB type is shown in Figure 2. This design of thick outer layers is not

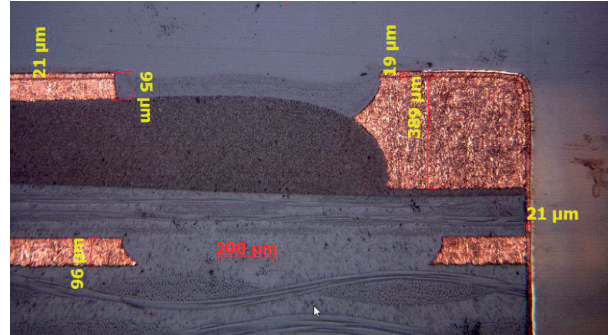


Figure 3 Cross section of PCB made by Iceberg technology with different thickness of conductive layer on outer side

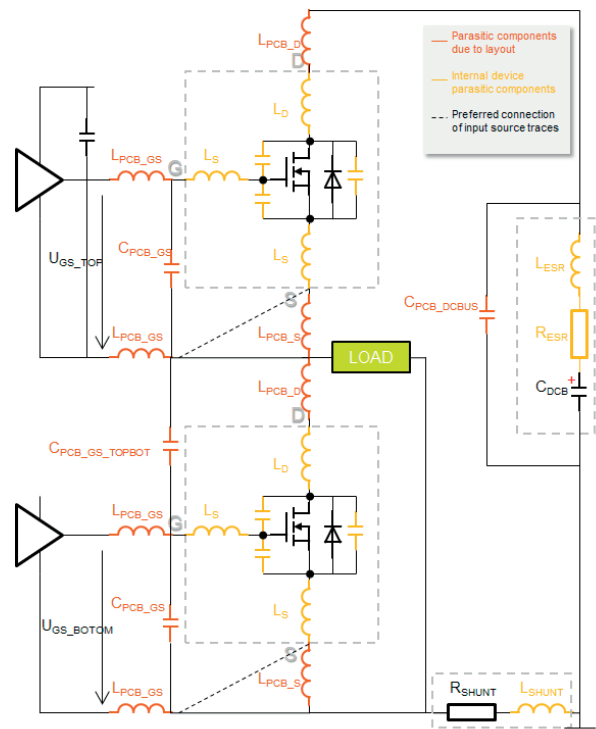


Figure 4 One branch of power inverter with parasitic components

suitable for combination of signal and power circuits together on the same side of PCB. The issues have occurred in the etching. The minimum distance of two conductive lines must be greater as for standard 70  $\mu\text{m}$  thickness of conductive layer.

Figure 3 partially shows the cross section of four layers PCB with implementation of two conductive layers with different thickness on the same outer layer of PCB. This way of integration of conductive layers makes possible to implement signal and power circuits on the same side of PCB. It is suitable design for compact devices.

Iceberg technology has also some disadvantages in real application. If the power layers of PCB are disproportionately overloaded and the conductive layers are suffering from high temperature, the PCB can be more susceptible to delamination.

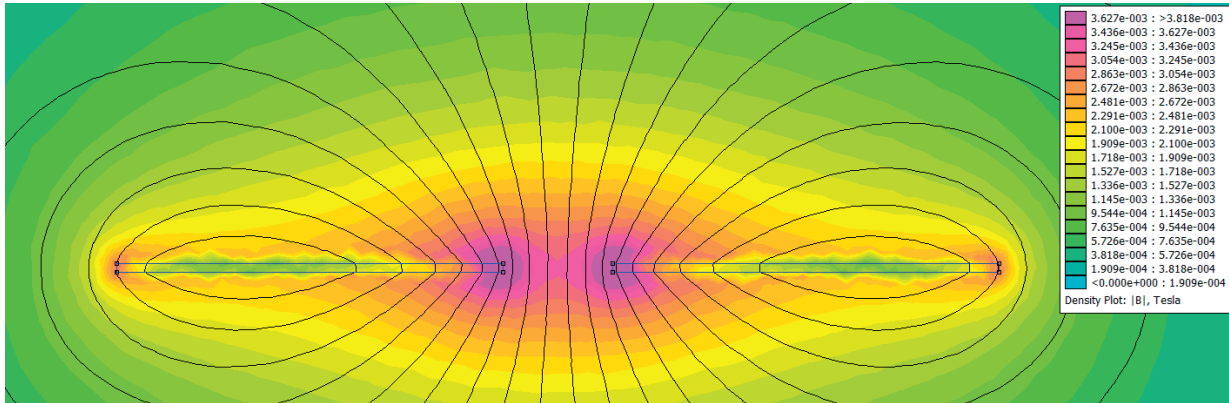


Figure 5 FEM analysis of coplanar leading of conductive lines PCB

The disadvantage of this technology is also in soldering of components on the thick layer. The heat is greatly depleted and soldering is complicated.

### 3. Influence of parasitic inductance in high current applications

The influence of parasitic parameters of the PCB in high current applications is more significant than standard low current applications. Combination of fast dynamic of switching and high value of controlled current can bring complications in the form of high voltage peaks, increased intensity of radiation and the decreasing of the efficiency.

Figure 4 shows one branch of 3-phase inverter with respecting parasitic components of the circuit. The aim of this chapter is to show and describe parasitic parameters of the power circuit and to find the solution for reducing these parameters.

Parasitic parameters of the components, MOSFETs, shunt resistor and DC link capacitors, are shown by yellow colour. There are parasitic inductances and capacitances of the power MOSFETs, parasitic inductance and equivalent serial resistance of the DC buss capacitor, and parasitic inductance of the shunt resistor. These parasitic parameters are affected by the manufacturer. Other parasitic parameters are affected by the layout. These parasitic inductances and capacitances are shown by red colour.

The inductance of the electric wire is defined as energy stored in the field and the value is determined by the current. It is necessary to reduce the trace inductance of PCB, due to the generating of high voltage peaks. This inductance can be directly reduced by increasing cross section area of the trace or decreasing the length of the trace. The thickness of the trace is limited by standards, therefore the cross section can be increased by the width of the trace.

The parasitic inductance of the source trace  $L_{PCB,S}$  and parasitic inductance of the drain trace  $L_{PCB,D}$  are affected by the trace of power line and parasitic inductances of the gate-source

loop  $L_{PCB,GS}$  are affected by routing the gate and source traces to MOSFETs. The parasitic inductance of gate traces is mitigated by minimizing of vias in gate-source loop, minimizing of length of this loop and making gate source traces wider. In case of insufficient mitigating of parasitic inductance of gate-source loop, the capacitor  $C_{PCB,GS}$  is added.

Figure 5 shows FEM analysis of two standard leading conductive lines. This arrangement of conductive lines is usually used in low current design of PCB. Due to the influence of magnetic flux, this layout of power lines is not suitable for high current applications. The total parasitic inductance of power lines is 23 nH, and these two conductive layers are coupled by inductive linkage with coincident direction. The magnetic flux density in the coplanar arrangement has maximum value in the place of the minimum distance of two power lines, see in Figure 5. In this case, emissions of magnetic flux to surroundings increases parasitic inductance. The magnetic flux density value is determined by current and distance of these two layers.

The following arrangement of conductive traces allows reducing the influence of parasitic inductance in the design. Figure 6 shows analysis of parallel leading of conductive traces. In this case, total parasitic inductance of power lines is 2.4 nH. Inductance of this arrangement is much smaller than in coplanar arrangement of power lines. Maximum value of magnetic flux density is generated between power lines and the value is determined by current and distance of two layers. The emission of magnetic flux to surrounding is lower in comparison with coplanar arrangement so parasitic inductance is lower too. Main benefit of parallel arrangement is compensation transient state by opposite layer.

All conductive traces of the design, gate-source loops and power loop, should be routed in recommended arrangement. The conductive lines of the routed circuits, where the current loop is closed from source to the load and back to the source, are proposed to lead opposite each other. That means that the magnetic field generated by the current with the positive direction of flow in one conductive line will be suppressed by the magnetic field generated by current with the negative direction of flow.

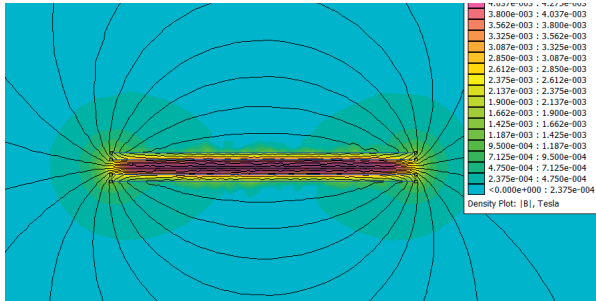


Figure 6 FEM analysis of parallel leading conductive lines of PCB

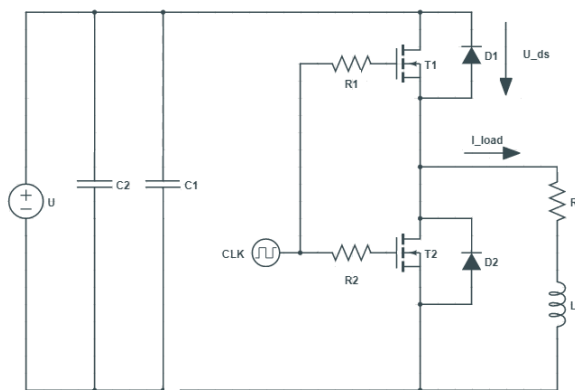


Figure 7 Schematic of half bridge power inverter for testing purpose

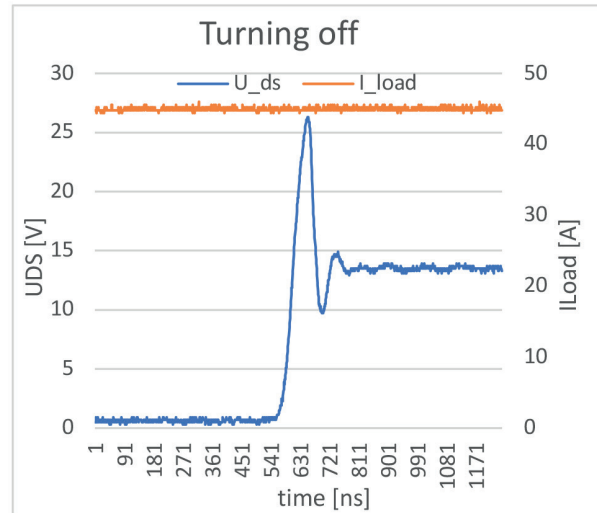
These two conductive layers are coupled by inductive linkage with anti-coincident direction.

#### 4. Quality comparison of switching for parallel and coplanar leading power lines

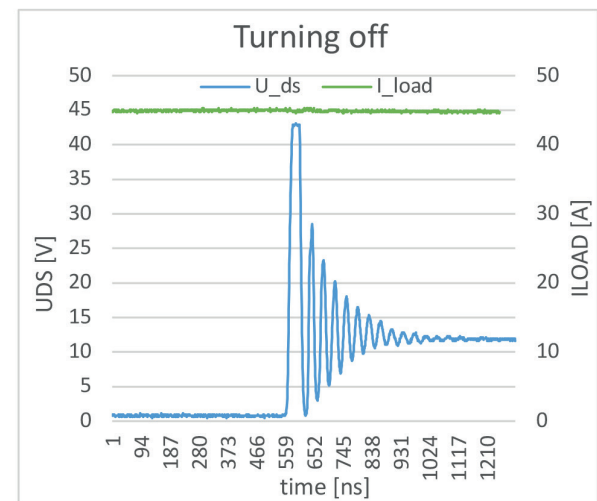
This chapter deals with comparison of switching quality for parallel and coplanar leading of power conductive traces. The testing of the switching was realized in one leg of 3 - phase power inverter, also known as a half bridge converter, shown in the Figure 7. The switching of power MOSFETs was realized in complementary mode. The voltage of top MOSFET transistor U<sub>DS</sub> was measured by differential probe and load current was measured by current probe.

The load was created by stator coils in the star connection, without neutral point, where the resistance of two coils is  $R = 0.014 \Omega$  and inductance of two coils is  $L = 20 \mu\text{H}$ .

The waveforms of drain-source voltage and load current are shown in the Figure 8. It is necessary to mention, that both of MOSFETs are switching, the snubbers are not realized in design, and therefore the voltage  $U_{DS}$  is oscillating. The aim of this chapter is to compare the influence of coplanar and parallel leading of power traces on the quality of MOSFET switching power, without



a)



b)

Figure 8 Waveforms of the  $U_{DS}$  of top transistor and load current for turn-off sequence a) parallel leading of power lines; b) coplanar leading of power lines

additional snubbers. Half-bridge converter is regulated to constant current of RL load.

Experimental results show different quality of switching the power MOSFET for coplanar and parallel leading of power traces. The influence of voltage  $U_{DS}$  oscillation is mitigated by parallel leading of power traces. The waveforms of voltage  $U_{DS}$  and load current are shown in Figure 8a). In the coplanar leading of power traces, the oscillation of voltage  $U_{DS}$  is considerable. In this case, the oscillation of voltage  $U_{DS}$  may be mitigated by the design of suitable snubbers [8]. In both case, the load current is the same and the axis of load current is on the opposite side as axis of voltage  $U_{DS}$ .

## 5. Conclusion

This paper presents two possible ways of high current PCB designs and their influence on the switching quality. The suitable technique for manufacturing high current PCB with signal and power layer on the same side of PCB was described. The power line of high current board is possible to lead by coplanar or parallel way. The experimental results show better quality of switching for parallel leading of power trace. In this case the electromagnetic interference will be lower in comparison with coplanar leading power trace. The following steps will be related to the efficiency analysis of losses, and it will be published later.

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