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SILICON NITRIDE BASED NON-VOLATILE MEMORY STRUCTURES WITH EMBEDDED Si OR Ge NANOCRYSTALS

Memory structures with an embedded sheet of separated Si or Ge nanocrystals were prepared by low pressure chemical vapour deposition using a Si_3N_4 control and SiO_2 tunnel layers. It was obtained that a properly located layer of semiconductor nanocrystals can improve both the charging and retention behaviour of the MNOS structures simultaneously. Memory window width of above 6 V and retention time of 272 years was achieved for charging pulses of ±15 V, 10 ms.

1. Introduction

Information storage in non-volatile memories is based on changing the threshold voltage of memory field effect transistors (FETs) by appropriate voltage pulses. The actual mechanism is injection of charge by tunneling and its storage in a floating gate, or in traps in metal-nitride-oxide-semiconductor (MNOS) or silicon-oxide-nitride-oxide-silicon (SONOS) devices located in the nitride layer close to the SiO_2/Si_3N_4 interface [1–8].

Nowadays memory arrays are based mainly on floating gate FETs. The reduction of dimensions is limited in these devices mainly due to reliability problems connected with defects in the thin oxide layer below the floating gate (tunnel oxide). The main problem is that through defects or weak points in tunnel oxide with reduced thickness the whole amount of stored charge carrying the information can be lost [1,6–8].

One of the possible solutions is to replace floating gate with separated semiconductor nanocrystals (NCs), which are electrically isolated. In this case the loss of information via local defects can be avoided [3–8].

Another possible way to avoid the above difficulties is the application of SONOS or MNOS devices. In these structures the charge holding the information is stored in the traps of nitride layer, which are electrically isolated by their nature. So, the effect of local defects in the tunnel oxide is reduced significantly [4,7–9].

Our group realized that formation of semiconductor NCs in nitride based memory structures can enhance both the charging and retention behaviour due to making direct tunneling possible to NCs and creating deep energy states, respectively. So, our idea was to realize MNOS structures with Si or Ge NCs at the Si_3N_4/SiO_2 interface [8–10]. Although two earlier works were devoted to the study the effect of semiconductor NCs in SONOS structures [9, 11], to the best of our knowledge we are the only group studying this effect in MNOS structures.

2. Experiment

For tunnel layer a SiO_2 layer was prepared after cleaning the wafers in 1 wt% HF. The SiO_2 layer was prepared using a HNO_3 treatment [12]; n-type Si wafers were immersed in 68 wt% HNO_3 at the boiling temperature (121 °C) for 60 minutes. This method yielded a SiO_2 layer with a thickness of 2.5 nm, as obtained by cross-sectional transmission electron microscopy [13].

The Si NC layer and the Si_3N_4 control layer were deposited by LPCVD on n-type Si substrates at 830 °C at a pressure of 30 Pa using SiH_2Cl_2 and NH_3. The Si_3N_4 layers were grown at gas flow rates of SiH_2Cl_2 and NH_3 of 21 and 90 sccm, respectively, while the Si NC layer with a gas flow rate of SiH_2Cl_2 of 100 sccm. The duration of deposition for the Si NC layer was 30 s and 60 s. Reference structures without Si NC layer were also prepared. Si_3N_4 control layer for structures with Si NCs was grown during 15 min, which yielded a layer thickness of 37–40 nm, obtained by ellipsometry.

In the MNOS structures with embedded Ge NCs the effects of duration of Ge NC deposition were studied as well (25 s and 50 s). Ge nanocrystals were deposited by electron beam evaporation at 350 °C [14]. The thickness of the control Si_3N_4 layer was about 35 nm. Reference devices without any Ge nanocrystal layers were also prepared.

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For electrical and memory measurements Al capacitors were formed with dimensions of 0.8 mm by 0.8 mm by evaporation. For backside ohmic contact also Al was evaporated after an appropriate chemical surface treatment [15].

The crystal structure of the layers was studied by X-ray photoelectron spectroscopy (XPS). Memory window and retention measurements were carried out on the capacitors. In this case the appropriate parameter for the characterisation of the memory effect and retention behaviour is the shift of flat-band voltage of capacitor. Memory window measurements were performed using voltage pulses with amplitude in range ±3 to ±25 V and width in range 10 ms to 400 ms. To enhance the development of the inversion layer, and so to avoid high voltage drop on the deep depletion layer during negative voltage pulses, the structures were illuminated with white light during memory window measurements. Retention measurements were performed in dark.

3. Results and Discussion

XPS results obtained on the MNOS structures after removing the upper part of the control silicon nitride layer clearly indicate the presence of NCs at the oxide/nitride interface, as it is presented in Fig. 1 for the structures with Si NC deposition duration of 30 s and 60 s. The Si NC peak is much more pronounced for a deposition duration of 60 s, than for 30 s, as it was expected.

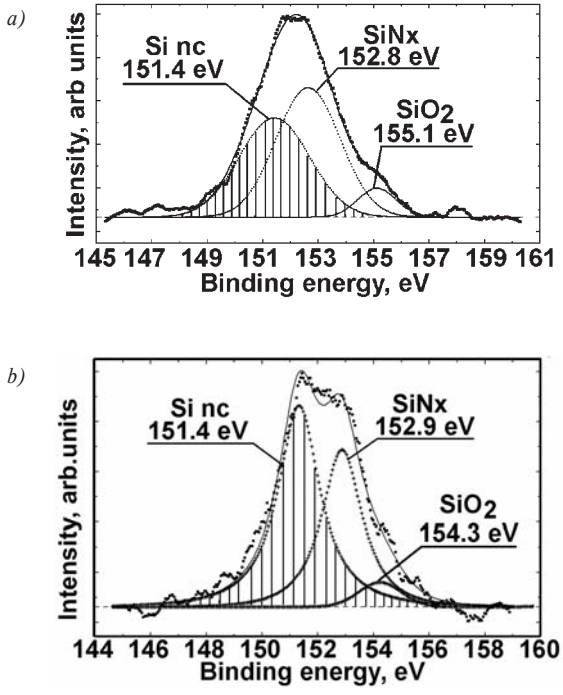

Fig. 1. Si 2s photoelectron spectrum of MNOS structures with Si nanocrystal deposition duration of 30 s (a) and 60 s (b) after Ar ion etching at depth of 38 nm.

The results of memory window measurements as a function of charging pulse amplitude with pulse width of 10 and 150 ms are presented in Fig. 2 for structures with Si nanocrystal deposition duration of 60 s. For longer charging pulses a wider memory window was obtained. The effect of Si NC deposition on the memory window is demonstrated in Fig. 3, which presents the memory window width for structures with Si nanocrystal deposition duration of 30 s and 60 s, and without middle NC layer deposition (indicated as 0 s duration), as a function of charging pulse amplitude. The structures with Si NCs exhibited a wider memory window for the whole studied voltage range than the reference structure.

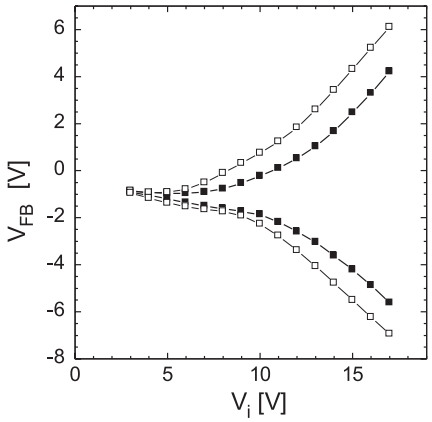

Fig. 2. The position of a memory window as a function of writing/erasing pulse amplitude with the pulse width of 10 ms (filled dots) and 150 ms (open dots) for the studied MNOS structures with Si nanocrystal deposition duration of 60 s. The upper curves are obtained for positive, the lower curves for negative voltage pulses.

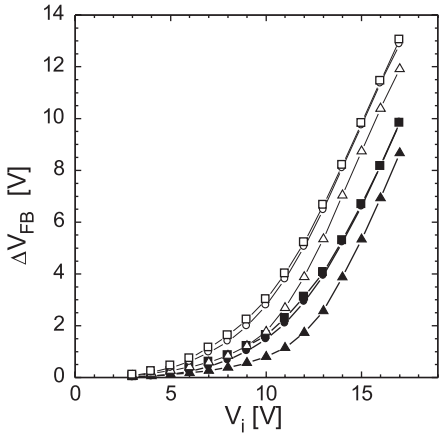

Fig. 3. The memory window width as a function of writing/erasing pulse amplitude with the pulse width of 10 ms (filled dots) and 150 ms (open dots) for the studied MNOS structures with Si nanocrystal deposition duration of 0 s (triangles), 30 s (circles), and 60 s (squares).

Retention behaviour is determined on the basis of flat-band voltage shift as a function of time after the application of a charg-

ing pulse. This shift of flat-band voltage is due to the loss of charge holding the information, through the tunnel and/or control layer. The shift exhibits logarithmic dependence on the time. So, plotting flat-band voltage as a function of the logarithm of time, a linear relation is obtained. The retention time (the time necessary to the lost of information) or the width of memory window after a certain time can be extrapolated from this linear relation fitted to the experimental data points [10]. Results concerning the retention behaviour of the studied structures with Si NCs are presented in Table 1. It is seen that the presence of Si NCs decreased the retention time, but for the samples with NC deposition of 30 s the memory window width after 10 years is still detectable. The extrapolation of flat-band voltage shift yielded a retention time of 41 years for these samples. It is even much higher than the standard requirement of 10 years.

The initial and extrapolated from the retention measurements for 1 and 10 years memory window widths for the studied structures. The charging pulse amplitude was ±15 V, the pulse width 10 ms — Tab. 1.

Nano-crystal	Nano-crystal deposition duration (s)	Initial memory window width (V)	Extrapolated memory window after 1 year (V)	Extrapolated memory window after 10 years (V)	Retention time (years)
Si	0	5.34	0.87	0.46	128
Si	30	6.61	0.85	0.32	41.2
Si	60	6.68	0.47	0	7.37
Ge	0	5.81	0.72	0.22	27.0
Ge	25	6.31	1.14	0.67	272
Ge	50	6.12	0.25	0	2.64

The results of memory window measurements of MNOS structures with Ge nanocrystals as a function of writing/erasing pulse amplitude with pulse width of 100 ms are presented in Fig. 4. The memory window is somewhat wider for memory structures with NCs than in the reference sample. However, while in the structures with Si NCs a longer deposition duration of NCs yielded a wider memory window, in the structures with Ge NCs the memory window is wider for a shorter deposition time.

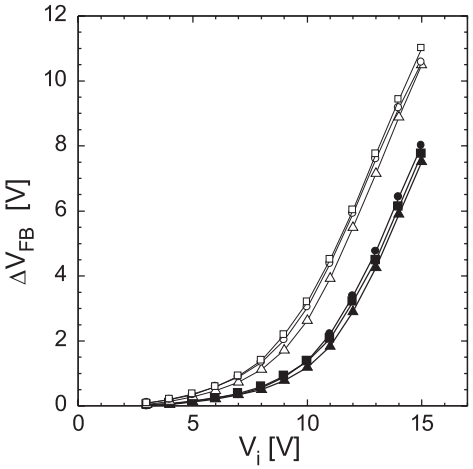

Fig. 4. The memory window width as a function of writing/erasing pulse amplitude with the pulse width of 10 ms (filled dots) and 150 ms (open dots) for the studied MNOS structures with Ge nanocrystal deposition duration of 0 s (triangles), 25 s (circles), and 50 s (squares).

The retention behaviour of the structures with Ge NCs is also summarized in Table 1. The best retention time of 272 years was obtained for Ge NC deposition duration of 50 s. It is very important that both injection and retention performances of samples with deposition duration of 50 s are better than those for reference samples without NCs. This demonstrates that a sheet of semiconductor NCs can improve both the injection and retention behaviour of silicon nitride based memory devices simultaneously [7,8].

4. Summary

MNOS structures with embedded Si or Ge nanocrystals were prepared by LPCVD and studied by memory window and retention measurements. Both the memory window and retention depended on the presence and deposition duration of nanocrystals. The presence of nanocrystals increased the memory window width, and enhanced in some cases the retention behaviour as well. The results demonstrate that a sheet of semiconductor nanocrystals can improve both the injection and retention behaviour of silicon nitride based memory devices.

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